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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/663,657	AWAKURA ET AL.	
	Examiner	Art Unit	
	WILLIAM BODDIE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *11-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, March 8th, 2011 the Applicants amended claims 1 and 10. Currently claims 1-10 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 11th, 2011 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizuka et al (US 7,274,363) in view of Sandoe et al. (US 6,243,061).

With respect to claim 1, Ishizuka discloses, a display apparatus comprising;

a pixel array including a plurality of pixels ($PL_{n,m}$ in fig. 15), each pixel including:

a light emitting unit (15 in fig. 2),

a drive element for controlling supply of a current to said light emitting unit (12 in fig. 2), and

a switching element (11 in fig. 2) for controlling said drive element according to an image signal (col. 1, line 63 – col. 2, line 18, for example);

a data signal drive circuit (24 in fig. 15) for receiving image data for each frame period and outputting said image signal to said pixel array based on said image data (col. 18, lines 5-9), said each frame period being provided for displaying one screen of said image data (fig. 5);

a scanning signal drive circuit (25 in fig. 15) for outputting a scanning signal to said pixel array, said scanning signal being for controlling a timing at which said switching element receives said image signal (col. 18, lines 1-4); and

a current source (27 in figs. 15-16) for, through said drive element (fig. 2, for example), outputting said current supplied to said light emitting unit (col. 18, lines 21-23).

Ishizuka does not expressly disclose, a control circuit for increasing a voltage applied to said light emitting unit while pixels with small gray scale numbers are emitting no light and pixels with large gray scale numbers are emitting light within said each frame period.

Sandoe discloses, a control circuit (20 in fig. 1) for continuously increasing a voltage (S+ and S- in fig. 11a-b) applied to a light emitting unit (15 in fig. 1) while pixels with small gray scale numbers are emitting no light and pixels with large gray scale

numbers are emitting light within said each frame period (col. 11, lines 28-64; figs. 11C-E represent black, gray and white gray scales, it should be clear from comparison to figs. 11a-b, that as the gray scale increases so does the ramp voltage on r and r+1).

Sandoe and Ishizuka are analogous art because they are from the same field of endeavor namely flat panel driving control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the increased voltage during brighter subframes taught by Sandoe in the subframes (fig. 5) of Ishizuka.

The motivation for doing so would have been to provide a smaller, simpler and less power consuming display (Sandoe; col. 11, lines 23-27).

With respect to claim 2, Ishizuka and Sandoe disclose, the display apparatus as claimed in claim 1 (see above).

Ishizuka further discloses, wherein:

said pixel array includes a pixel for red, a pixel for green, and a pixel for blue (col. 13, lines 32-45, for example); and

said current source is provided for each of said pixel for red, said pixel for green, and said pixel for blue separately (fig. 9).

With respect to claim 3, Ishizuka and Sandoe disclose, the display apparatus as claimed in claim 1 (see above).

Ishizuka further discloses, wherein said current source controls said value or said amount of said current according to a control signal input to said current source (col. 18, lines 46-63; control signal judging indicates how much current offset to apply).

With respect to claim 5, Ishizuka and Sandoe disclose, the display apparatus as claimed in claim 3 (see above).

Ishizuka further discloses, a voltage control circuit (32-36 in fig. 16) for detecting said value or said amount of said current (col. 18, lines 34-45) and, based on said value or said amount of said current, generating said control signal input to said current source (col. 18, lines 46-67).

With respect to claim 10, Ishizuka discloses, a method for display an image based on image data by use of a pixel array including a plurality of pixels ($PL_{n,m}$ in fig. 15), each pixel including:

a light emitting unit (15 in fig. 2);

a drive element for controlling supply of a current to said light emitting unit (12 in fig. 2); and

a switching element (11 in fig. 2) for controlling said drive element according to an image signal (col. 1, line 63 – col. 2, line 18, for example);

wherein said method comprises the steps of:

outputting said current from said current source to said light emitting unit through said drive element (col. 18, lines 21-23);

receiving said image data for each frame period and outputting said image signal from a data signal drive circuit to said pixel array based on said image data (col. 18, lines 5-9), said each frame period being provided for displaying one screen of said image data (fig. 5);

outputting a scanning signal from a scanning signal drive circuit (25 in fig. 15) to said pixel array, said scanning signal being for controlling a timing at which said switching element receives said image signal (col. 18, lines 1-4).

Ishizuka does not expressly disclose, increasing a voltage applied to said light emitting unit while pixels with small gray scale numbers are emitting no light and pixels with large gray scale numbers are emitting light within said each frame period.

Sandoe discloses, continuously increasing a voltage (S+ and S- in fig. 11a-b) applied to a light emitting unit (15 in fig. 1) while pixels with small gray scale numbers are emitting no light and pixels with large gray scale numbers are emitting light within said each frame period (col. 11, lines 28-64; figs. 11C-E represent black, gray and white gray scales, it should be clear from comparison to figs. 11a-b, that as the gray scale increases so does the ramp voltage on r and r+1).

Sandoe and Ishizuka are analogous art because they are from the same field of endeavor namely flat panel driving control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the increased voltage during brighter subframes taught by Sandoe in the subframes (fig. 5) of Ishizuka.

The motivation for doing so would have been to provide a smaller, simpler and less power consuming display (Sandoe; col. 11, lines 23-27).

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizuka et al (US 7,274,363) in view of Sandoe et al. (US 6,243,061) and further in view of Hack et al. (US 2002/0030647).

With respect to claim 4, Ishizuka and Sandoe disclose, the display apparatus as claimed in claim 3 (see above).

Ishizuka further discloses generating said control signal input to said current source (col. 18, lines 46-67).

Neither Sandoe nor Ishizuka expressly disclose a PWM control circuit.

Hack discloses, a PWM control circuit for generating a PWM control signal for, through said drive element, controlling whether or not said light emitting unit emits light, during said each frame period (para. 49); and

a voltage control circuit for, based on said PWM control signal, generating said control signal input to said drive source (para. 49; PWM method will involve measuring/storing OLED current versus PWM amount).

Hack, Sandoe and Ishizuka are analogous art because they are both from the same field of endeavor namely current detection and driving circuitry of flat panel displays.

At the time of the invention it would have been obvious to one of ordinary skill in the art to control the pixels via PWM and to alter the current source of Ishizuka as taught by Hack.

The motivation for doing so would have been to for well-known benefit of increased display uniformity as individual pixel element differences are not as noticeable.

4. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizuka et al (US 7,274,363) in view of Sandoe et al. (US 6,243,061) and further in view of Kimura et al. (US 6,518,962).

With respect to claim 6, Ishizuka and Sandoe disclose, the display apparatus as claimed in claim 5 (see above).

Ishizuka further discloses generating said control signal input to said current source (col. 18, lines 46-67).

Neither Sandoe nor Ishizuka expressly disclose that the control circuit calculates a luminance level of the image data.

Kimura discloses, wherein a voltage control circuit (21b, 18 in fig. 10) calculates a luminance level of image data (col. 35, line 66 – col. 36, line 17) for each frame period (207 in fig. 17) based on a value or an amount of current (output of 16' in fig. 17) and, based on said luminance level of said image data for said each frame period (col. 36, lines 4-15), generating a control signal (output of 209 in fig. 17) input to a driving source (200a in fig. 17).

Kimura, Sandoe and Ishizuka are analogous art because they are both from the same field of endeavor namely flat panel display control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to calculate the luminance level and to alter the current source of Ishizuka as taught by Kimura.

The motivation for doing so would have been to correct for deterioration over time thereby achieving a higher quality display for a longer period of time (Kimura; col. 1, lines 65-67).

With respect to claim 7, Ishizuka and Sandoe disclose, the display apparatus as claimed in claim 5 (see above).

Ishizuka further discloses generating said control signal input to said current source (col. 18, lines 46-67).

Neither Sandoe nor Ishizuka expressly disclose that the control circuit calculates a degree of degradation of the light emitting unit.

Kimura discloses, wherein a voltage control circuit (21b, 18 in fig. 10) calculates the degree of degradation of a light emitting unit (15 in fig. 10) based on a value or an amount of current (Idm in fig. 10) and, based on said degree of degradation of said light emitting unit (col. 36, lines 1-17), generating a control signal (output of 21b in fig. 10) input to a driving source (13, 22a in fig. 10).

At the time of the invention it would have been obvious to one of ordinary skill in the art to calculate the degree of degradation and to alter the current source of Ishizuka as taught by Kimura.

The motivation for doing so would have been to correct for deterioration over time thereby achieving a higher quality display for a longer period of time (Kimura; col. 1, lines 65-67).

5. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizuka et al (US 7,274,363) in view of Sandoe et al. (US 6,243,061) and further in view of Tsuruoka et al. (US 6,414,443).

With respect to claim 8, Ishizuka and Sandoe disclose, the display apparatus as claimed in claim 5 (see above).

Ishizuka further discloses generating said control signal input to said current source (col. 18, lines 46-67).

Neither Sandoe nor Ishizuka expressly disclose that the control circuit calculates a temperature of the light emitting unit.

Tsuruoka discloses, wherein a voltage control circuit (35 in fig. 4) calculates temperature of said pixel array based on said value or said amount of said current (col. 4, lines 25-36) and, based on said temperature of said pixel array, generating a control signal (output of 34 in fig. 4) input to a driving source (33 in fig. 4).

Sandoe, Tsuruoka and Ishizuka are analogous art because they are both from the same field of endeavor namely flat panel display control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to calculate the temperature and to alter the current source of Ishizuka as taught by Tsuruoka.

The motivation for doing so would have been to correct for deterioration over time thereby achieving a higher quality display that is independent of temperature variations (Tsuruoka, col. 2, lines 16-18).

With respect to claim 9, Ishizuka and Sandoe disclose, the display apparatus as claimed in claim 3 (see above)

Neither Sandoe nor Ishizuka expressly disclose another light emitting unit separate from the array or a control circuit for detecting temperature.

Tsuruoka discloses, a light emitting unit (10' in fig. 4) provided separately from a pixel array (10 in fig. 4); and

a voltage control circuit (35 in fig. 4) for detecting temperature of said another light emitting unit (col. 4, lines 25-36) and, based on said temperature of said another light emitting unit, generating a control signal (output of 34 in fig. 4) input to a driving source (33 in fig. 4).

At the time of the invention it would have been obvious to one of ordinary skill in the art to calculate the temperature and to alter the current source of Ishizuka as taught by Tsuruoka.

The motivation for doing so would have been to correct for deterioration over time thereby achieving a higher quality display that is independent of temperature variations (Tsuruoka, col. 2, lines 16-18).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM BODDIE whose telephone number is (571)272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William L Boddie/
Primary Examiner, Art Unit 2629
8/26/2011